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buffers + (transfer or move) + (entry or element or lane or line)

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J Heinlein, K Gharachorloo, S Dresser, A Gupta, ... - ACM SIGOPS Operating Systems Review, 1994 - portal.acm.org

... its dedicated data paths to efficiently **transfer** data while ... These **buffers** form an array of cache **line** sized reg ... is implemented as a single **entry** that represents ...Cited by 70 - [Web Search](#) - [portal.acm.org](#) - [www-flash.stanford.edu](#) - [www-flash.stanford.edu](#)A design space and design rules for user interface software architecture

TG Lane, PDF File, PS File - 1990 - sei.cmu.edu

... DTIC provides access to and **transfer** of scientific and ... of expressing software engineering knowledge [Lane 90b ... physical interpretations (eg, "draw **line**," but not ...Cited by 8 - [View as HTML](#) - [Web Search](#) - [sei.cmu.edu](#) - [sei.cmu.edu](#) - all 4 versions » - [Library Search](#)The Stanford FLASH Multiprocessor

J Kuskin, D Ofelt, M Heinrich, J Heinlein, R ... - ISCA, 1994 - portal.acm.org

... contains a specialized data path optimized to **move** data between ... and a base block-**transfer** protocol we have designed for ... cessor, a link to the next **entry** in ...Cited by 489 - [Web Search](#) - [vlsi.csl.cornell.edu](#) - [pag.lcs.mit.edu](#) - [cs.fau.de](#) - all 21 versions »MECHANICAL SYSTEM FOR ON-LINE FRUITS SORTING AND GRADING USING MACHINE VISION TECHNOLOGY

SM Iqbal, D Ganesan, PS Rao - isu.iisc.ernet.in

... The ball nut continues to **move** down until it contacts the spindle frame. ... This gives the **line** scan camera a clear view of the apple cheek. ...[View as HTML](#) - [Web Search](#)BRIDGE ARCHITECTURE, PERFORMANCE, AND MANAGEMENT

N Linge, E Ball, R Tasker, P Kummer - Telecommunications, 1989. Second IEE National Conference on, 1989 - ieeexplore.ieee.org

... access protocols and are able to **transfer** frames to ... The remaining **buffers** constitute the frame transmission queues ... for end-stations apparently to **move** from one ...[Web Search](#) - [ieeexplore.ieee.org](#)Technical Research Report

G Atallah, M Ball, J Baras, S Goli, R Karne, S ... - techreports.isr.umd.edu

... As an example, the operator can **move** a "slider ... E1 rates, employing the Asynchronous **Transfer** Mode (ATM ... packets, ODLC link downs, and Inroute/Outroute **Buffers**. ...[View as HTML](#) - [Web Search](#)Mechanisms Involved In Target Sequence Recognition AND Integration OF Human LINE-1 Retrotransposons

N Zingler - chemie.uni-hamburg.de

... 2.4.8.2 **Transfer** of DNA onto nylon membranes ... HGWD human genome working draft kb kilobasepairs kDa kilodalton L1 the human **LINE-1** **element** **LINE** long interspersed ...[View as HTML](#) - [Web Search](#) - [chemie.uni-hamburg.de](#)Achieving holonic control-an incremental approach.

J Jarvis, D Jarvis, D McFarlane - Computers in Industry, 2003 - agent-software.com

... Two **buffers**, which presents ... The table can **move** between two positions - one with jig1 adjacent ... the CNC axes, the chuck, the spindle, the **transfer** mechanism or ...



data + buffers + (transfer or move)

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[IBM Tivoli Storage Manager for AIX: Administrator's Reference ...](#)

MOVE NODEDATA (**Move Data** by Node in a Sequential Access Storage Pool) ...

RESET BUFPOOL (Reset the Database **Buffer** Pool Statistics) ...

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[Technology | Mammoth | Adaptive **Data** Buffering - Exabyte](#)

Streaming occurs when the **data transfer** rate to or from the host closely matches

the tape ... MammothTape™ technology's **data buffer** is also adaptive. ...

www.exabyte.com/technology/mammoth/intro/adaptivedatabuffering.cfm - 43k - [Cached](#) - [Similar pages](#)

[Message Transfer Agent Tuning](#)

Additionally, X.400 connectors and mailbox **move** operations require the MTA. ...

DB **data buffers** per object This value is the number of database server ...

www.microsoft.com/.../exchange/guides/E2k3Perf_ScalGuide/d3c91edc-a5b7-4620-97f1-ef3c37c3a3a1.mspx - 23k -

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tions that create the need to **move data** extended distances over Fibre Channel links.

... If congestion on the PCI bus occurs, the HBA **data buffer** can serve ...

www.emulex.com/products/white/fc/buffer.pdf - [Similar pages](#)

[a scsicmd\(8\) command table for use with an EXB-210 tape library ...](#)

COMMAND: **move** medium (**move**): CMD_WRITE CDB: command descriptor block (cdb): 12

... number of **data transfer** elements (ndte) **BUFFER** + 24: transport geometry ...

cns.utoronto.ca/~pkern/stuff/exb-210.scsicmd - 9k - [Cached](#) - [Similar pages](#)

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Internal **transfer** rate is the rate at which a drive can **move** ... Increasing the

cache **buffer** segment size, which will maximize the **data** prefetch feature of ...

www.seagate.com/support/kb/disc/av.html - 19k - [Cached](#) - [Similar pages](#)

[HP 3000 Manuals](#)

Data Transfer Method D This **data transfer** method lets you **move data** to and from the

... Use this **transfer** method when the application **data buffer** does not ...

docs.hp.com/cgi-bin/doc3k/B3242490002.10134/31 - 8k - [Cached](#) - [Similar pages](#)

[Central processing unit with improved stack register operation](#)

The internal **data** bus D is connected, through a **data buffer** memory (DB) 31, ...

After the time t.sub.2, when the **data transfer** instruction **MOVE** and the ...

www.freepatentsonline.com/us5001629.html - 41k - [Cached](#) - [Similar pages](#)

[Embedded.com - The best way to **move** multimedia **data**](#)

For example, the DMA controller might be optimized to **transfer** a **data** word on

... These functions help ensure that **data buffers** do not overflow due to DMA ...

www.embedded.com/showArticle.jhtml?articleID=16700107 - 96k - [Cached](#) - [Similar pages](#)

[New **Data Transfer** Capabilities](#)

One of the new capabilities now available is improved **data transfer** ... Now that

you have some background information, let's **move** on to some real code. ...

java.sun.com/developer/technicalArticles/releases/data/ - 46k - [Cached](#) - [Similar pages](#)



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FM 101-5-1, Operational Terms and Graphics, Chapter 1, J,K,L

lane - A route through an enemy or friendly obstacle that provides a passing ...

line of demarcation (LOD) - A **line** defining the boundary of a **buffer zone** ...

www.fas.org/man/dod-101/army/docs/fm101-5-1/f545-jk.htm - 38k - [Cached](#) - [Similar pages](#)

Untitled Document

Add one standard **lane** each direction: County **Line** to Milpas ... Corridor to more efficiently regulate the **entry** of 101 traffic and **buffer** freeway flow from ...

www.101inmotion.com/glossary/glossary.html - 42k - [Cached](#) - [Similar pages](#)

The Stanford FLASH Multiprocessor

For efficiency, the first **element** of the sharer list is stored in the directory

... Staging data through data **buffers** allows the data **transfer** logic to ...

www.flash.stanford.edu/architecture/papers/ISCA94/ - 66k - [Cached](#) - [Similar pages](#)

Integration of Message Passing and Shared Memory in the Stanford ...

... as a single **entry** that represents the head **element** in the queue. ... Loading the next memory **line** into the second **buffer** where the first left off will ...

www-flash.stanford.edu/architecture/papers/flash_msg/ - 99k - [Cached](#) - [Similar pages](#)

UDP Minutes for Wednesday, May 26, 2004

Elevators are in glass to bring light down to the **entry** plaza. ... While some individual **elements** along the **lane** could be considered handsome, ...

www.city.vancouver.bc.ca/commsvcs/ planning/udp/2004/minutes/may26.htm - 39k - [Cached](#) - [Similar pages](#)

Chapter 9 Page 1 - Freeway Management and Operations Handbook

HOV facilities represent just one potential **element** for managing the surface ...

The two types of centers are on-**line**, which are located on the HOV **lane** and ...

ops.fhwa.dot.gov/freewaymgmt/ freeway_mgmt_handbook/chapter9_01.htm - 39k - [Cached](#) - [Similar pages](#)

%Z ...

This **lane** is implemented using a central ``floating'' deadlock **buffer** resource

... **transfer** and scattering in one step, reading the data **elements** with some ...

www.cs.wisc.edu/arch/www/ISCAbib/isca22.refer - 51k - [Cached](#) - [Similar pages](#)

[PPT] Lecture 1: Course Introduction and Overview

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Scalar registers: single **element** for FP scalar or address ... multiple queues to **transfer** from memory **buffer** to registers; check last address in queues ...

american.cs.ucdavis.edu/academic/ecs201a/fred/l5.ppt - [Similar pages](#)

HCM Glossary

Crown **Line**. A **lane** marking that connects from the entrance gore area directly

... median area in a first **move**, then completing the **entry** with a second **move**. ...

www.aattraffic.com/HCMGlossary.htm - 94k - [Cached](#) - [Similar pages](#)

JVI -- Nugent et al. 73 (1): 427

Lane P contains 0.35 fmol of full-length probe RNA, and lanes 1 to 14 ... type 1 and/or type 2 internal ribosomal **entry** site **elements**: genetic hybrids and ...

jvi.asm.org/cgi/content/full/73/1/427 - [Similar pages](#)



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Norman Meyrowitz, Andries van Dam

September 1982 **ACM Computing Surveys (CSUR)**, Volume 14 Issue 3

Full text available: pdf(9.17 MB)

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2 [Three-dimensional medical imaging: algorithms and computer systems](#)

M. R. Stytz, G. Frieder, O. Frieder

December 1991 **ACM Computing Surveys (CSUR)**, Volume 23 Issue 4

Full text available: pdf(7.38 MB)

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Keywords: Computer graphics, medical imaging, surface rendering, three-dimensional imaging, volume rendering

3 [Integration of message passing and shared memory in the Stanford FLASH multiprocessor](#)

John Heinlein, Kourosh Gharachorloo, Scott Dresser, Anoop Gupta

November 1994 **Proceedings of the sixth international conference on Architectural support for programming languages and operating systems**, Volume 29, 28 Issue 11, 5

Full text available: pdf(1.80 MB)

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The advantages of using message passing over shared memory for certain types of communication and synchronization have provided an incentive to integrate both models within a single architecture. A key goal of the FLASH (FLEXible Architecture for SHared memory) project at Stanford is to achieve this integration while maintaining a simple and efficient design. This paper presents the hardware and software mechanisms in FLASH to support various message passing protocols. We achieve low overhead ...

4 [Piranha: a scalable architecture based on single-chip multiprocessing](#)

Luiz André Barroso, Kourosh Gharachorloo, Robert McNamara, Andreas Nowatzky, Shaz Qadeer, Barton Sano, Scott Smith, Robert Stets, Ben Verghese

May 2000 **ACM SIGARCH Computer Architecture News, Proceedings of the 27th annual international symposium on Computer architecture**, Volume 28 Issue 2

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1 [Efficient data-parallel files via automatic mode detection](#)

Jason A. Moore, Philip J. Hatcher, Michael J. Quinn

May 1996 **Proceedings of the fourth workshop on I/O in parallel and distributed systems: part of the federated computing research conference**Full text available: [pdf\(1.34 MB\)](#)Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)**2** [Input-Output Buffering and Fortran](#)

David E. Ferguson

January 1960 **Journal of the ACM (JACM)**, Volume 7 Issue 1Full text available: [pdf\(381.86 KB\)](#)Additional Information: [full citation](#), [index terms](#)**3** [The VMP network adapter board \(NAB\): high-performance network communication for multiprocessors](#)

H. Kanakia, D. Cheriton

August 1988 **ACM SIGCOMM Computer Communication Review , Symposium proceedings on Communications architectures and protocols**, Volume 18 Issue 4Full text available: [pdf\(1.63 MB\)](#)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

High performance computer communication between multiprocessor nodes requires significant improvements over conventional host-to-network adapters. Current host-to-network adapter interfaces impose excessive processing, system bus and interrupt overhead on a multiprocessor host. Current network adapters are either limited in function, wasting key host resources such as the system bus and the processors, or else intelligent but too slow, because of complex transport protocols and because of a ...

4 [Operating system benchmarking in the wake of Imbench: a case study of the performance of NetBSD on the Intel x86 architecture](#)

Aaron B. Brown, Margo I. Seltzer

June 1997 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1997 ACM SIGMETRICS international conference on Measurement and modeling of computer systems**, Volume 25 Issue 1Full text available: [pdf\(1.98 MB\)](#)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The *Imbench* suite of operating system microbenchmarks provides a set of portable programs for use in cross-platform comparisons. We have augmented the *Imbench* suite to

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S24	88	(variable near4 length) near4 (vliw or (long adj1 instruction\$1))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/05/13 15:30
S25	0	(vliw or (long adj1 instruction\$1)) near4 (syllable\$1 or sub?instruction\$1) near4 issu\$3 near4 buffer\$1	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/05/13 15:31
S26	0	(vliw or (long adj1 instruction\$1)) near4 (syllable\$1 or sub?instruction\$1) near4 issu\$3 near4 (buffer\$3 or cach\$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/05/13 15:31
S27	0	(vliw or (long adj1 instruction\$1)) near4 (syllable\$1 or sub?instruction\$1 or subinstruction\$1) near4 issu\$3 near4 (buffer\$3 or cach\$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/05/13 15:31
S28	0	((vliw or (long adj1 instruction\$1)) near4 (syllable\$1 or sub?instruction\$1 or subinstruction\$1)) with (issu\$3 near4 (buffer\$3 or cach\$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/05/13 15:32
S29	0	((vliw or (long adj1 instruction\$1)) near4 (syllable\$1 or sub?instruction\$1 or subinstruction\$1)) same (issu\$3 near4 (buffer\$3 or cach\$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/05/13 15:32
S30	3	((vliw or (long adj1 instruction\$1)) near4 (syllable\$1 or sub?instruction\$1 or subinstruction\$1)) same (issu\$3 with (buffer\$3 or cach\$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/05/13 15:33
S31	3	((vliw or (long adj1 instruction\$1)) near4 (syllable\$1 or sub?instruction\$1 or subinstruction\$1)) same (issu\$3 same (buffer\$3 or cach\$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/05/13 15:34
S32	3	((vliw or (long adj1 instruction\$1)) with (syllable\$1 or sub?instruction\$1 or subinstruction\$1)) same (issu\$3 same (buffer\$3 or cach\$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/05/13 15:34

S33	6	((vliw or (long adj1 instruction\$1)) same (syllable\$1 or sub?instruction\$1 or subinstruction\$1)) same (issu\$3 same (buffer\$3 or cach\$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/05/13 15:36
S34	3	vliw and (Sharanpani or Hall).in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/05/13 15:36
S35	13	vliw and (Sharangpani or Hall).in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/05/13 15:37
S36	1	vliw and (Sharangpani or Hall).in. and (stop adj1 bit\$1)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/05/13 15:37
S37	1	("20020144094").PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/08/11 17:02